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Non-Isolated Dual-Output Mirror-Symmetric DC-DC Converters: Topology Construction and Analysis

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Abstract: This paper proposes an improved series of a revolutionary mirror-symmetrical dual-output non-isolated dc-dc converter using the voltage lift approach. Its unique design offers a series of improvements that set it apart from traditional converters. The converter's basic architecture allows for substantial voltage transfer gains when converting dc-dc voltage, not just from positive to positive, but also from positive to negative. This flexibility sets it apart from other dual-output dc-dc converters currently available on the market.A key advantage of this converter is its simplicity. All suggested topologies employ a single power switch, eliminating the need for transformers or cascade connections. This simplicity could make it an attractive option for future practical applications. The shared ground design ensures more dependable dual-output voltages, further enhancing the converter's reliability.The theoretical foundation of this converter is rock solid, with a thorough topology analysis conducted for both discontinuous and continuous conduction modes. This analysis provides a solid foundation for understanding the converter's operation and its potential for real-world applications.To validate the suggested topologies, experimental results and simulations are presented. These results demonstrate the converter's effectiveness and confirm its theoretical advantages. They also highlight its adaptability to different operating conditions, making it a versatile solution for a range of dc-dc voltage conversion needs.

Keywords: DC-DC Converters, Dual-Output, Topology, Voltage Lift Technique, Voltage Transfer Gains

1. Introduction

Two distinct conversion paths make up a Dual-Output dc-dc converter, which can convert a positive input source voltage into both a positive and negative output voltage [1-3]. Telecommunications hardware, computer peripheral power supplies, differential servo motor drives, and certain symmetrical voltage medical devices are just a few examples of the industrial and computer peripheral applications that frequently use these devices. Research and application of this mirror-symmetric Dual-Output dc-dc power conversion technology are emerging as a significant and promising field, due to the quick advancement of modern science and technology.

By using transformer isolation and cascading connections, Dual-Output dc-dc converters with high voltage transmission gain can be created using standard dc-dc conversion techniques [4-9]. But these converters' numerous power switches and transformers not only significantly raise the control's complexity but also raise the circuit's expense. The transformer's magnetic flux and leakage inductance in particular have an impact on how the switchgear and output voltage are regulated. non-isolated Dual-Output dc-dc converters, which are frequently generated from traditional dc-dc topologies, can be an excellent option to solve the aforementioned issues. non-isolated Dual-Output converters, for instance, have been investigated using buck-boost and zero-inductance DC (ZETA) converters [10].

Because of their excellent qualities, SEPIC and Cûk converters in classical topologies have several industrial uses. It is possible to construct Dual-Output converters with them. Because of their different voltage transfer functions, SEPIC and Cûk converters may both execute step-down and step-up dc-dc conversions depending on the duty cycle D condition.

This topology for SEPIC converters does not show an output polarity inversion, and the voltage transfer gain is:

$$M_{SEPIC} = \frac{D}{1-D} \tag{1}$$

In the case of the Cûk converter, the output polarity is reversed, and the voltage transfer gain is:

$$M_{Cuk} = -\frac{D}{1-D} \tag{2}$$

Due to the influence of parasitic elements, there is a practical upper limit on the actual value of D (usually D < 0.9). As a result, the output voltage and power transfer efficiency of both converters are severely limited.

Advanced dc-dc conversion enhancement techniques have been extensively explored, including switched-capacitor (SC) and voltage boost (VL) techniques [11-17]. The goal of these technologies is to achieve high efficiency, high power density, and simple structure. Combining the classic prototype with the enhancements described above may help drive the adoption of non-isolated dual-output converters. The main advantage of SC technology is that it does not require the use of inductors, so it can achieve miniaturization and high power density.

VL technology is different from current SC technology which is an effective method to be applied in electronic circuit design, especially in radio engineering. It can also improve the performance and characteristics of dc-dc converters. In VL technology, both inductors and capacitors play an important role, and all internal capacitors are adequately charged by the power supply. In addition, the VL-type structure uses fewer power switches (typically a single switch or two synchronous switches) and avoids complex multiple switch control schemes. In this paper, we apply VL technology to the prototype of SEPIC and Cûk converters, and propose a new series of mirror-symmetrical dual-output transformer-free VL-type converters. They are divided into the following categories:

1) Dual-Output VL-type converter with mirror symmetry and self-lift circuit
2) boost enhanced series
3) super enhanced series

Positive to positive/negative dc-dc voltage increase conversion is made possible by the suggested architecture, which also has a simple construction, improved voltage transfer gain, power density, and efficiency. They use a single power switch and are unlike any other Dual-Output dc-dc boost converter on the market. Consequently, they have a wide range of uses in industrial settings and as computer peripherals, particularly in high output voltage projects. The ensuing sections will conduct a thorough topology study. The resulting formulas compute the capacitive voltage ripple, inductor current ripple, and boundary conditions.

For any of the components X in this article, their instantaneous current and voltage are stated as i_X and v_X. During a steady-state switching cycle, its average voltage and current are expressed as I_X and V_X. All reference directions for current and voltage can be referenced in the corresponding diagrams. In general, all the elements are ideal, and $V_oI_o=V_{in}I_{in}$ indicates that the output power equals the input power. The value at which the continuous conduction mode (CCM) and discontinuous conduction mode (DCM) meet is indicated by any parameter that has the subscript -B. The symbols ε, ζ, and ξ are defined as the output voltage change ratio, the inductor current change ratio, and the diode current change ratio, accordingly.

2. Mirror-Symmetrical Dual-Output VL-Type Converter

We contrast SEPIC and Cûk, two prototypes of dc-dc converter circuits. There are two components to every prototype: the source component and the pump component. The remaining components make up the pump part, while the voltage source, inductor L, and active switch S comprise the source part. As a result, every prototype can be thought of as a unique way for these two components to cascade together.

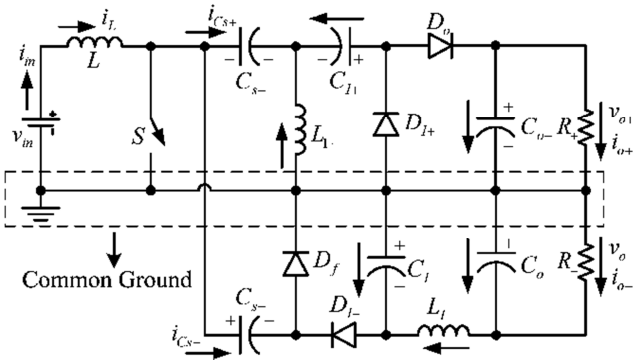


Figure 1. *Mirror-symmetrical Dual-Output VL-type converter topology.*

We integrate the source sections of the SEPIC and Cûk converters on the input side as they both have the identical source component (*L*-*S*) and a voltage transfer gain of the opposite polarity. Furthermore, capacitors and diodes were added at different locations in these two pump sections before they were combined. As shown in Figure 1, the newly acquired topology is referred to as a mirror-symmetrical dual-output VL converter. This is due to the fact that we have successfully implemented VL technology, which will be validated in the following topology analysis. As you can see, four new components, D_{l+}, D_{l-}, C_{l+}, and C_l-, have been added to the previous pump section.

Combining both positive and negative conversion routes, the topology suggested in this research is a hybrid of both. In the positive conversion path, the components include the source section $L-S$, pump section $C_{s+}-(S)-L_{l+}-D_{l+}-C_{l+}$, and output filter sections D_o-C_{o+}; in the negative conversion path, the components additionally include the source section $L-S$, pump section $C_{s-}-(S)-D_f$, and output Π-type filter sections $D_{l-}-C_{l-}-L_{l-}-C_{o-}$. This topology has a common ground, which allows the circuit to provide positive and negative voltages more reliably. In the following sections, we will

analyze the operation of this circuit in detail and assume that the circuit operates in CCM (Continuous Conduction Mode).

2.1. Positive Conversion Path

The switching diagrams in Figure 3 display the main steady-state waveforms, with reference directions taken from Figure 1. It can be observed that in the steady state, the average voltage across *L* over a cycle is zero. Therefore,

$$V_{Cs+} = V_{in} \tag{3}$$

During the process of turning on, the voltage across C_{1+} is the same as the voltage across V_{Cs+}. Given that the values of C_{s+} and C_{1+} are significantly large, we have:

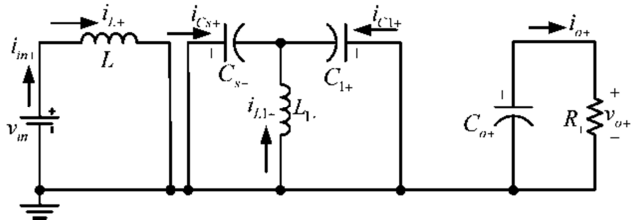
$$V_{C1+} = V_{Cs+} = V_{in} \tag{4}$$

When turning on, the inductor current i_L rises, and when turning off, it falls. The corresponding voltages across *L* are V_{in} and $-(V_{Co+} - V_{C1+} - V_{in} + V_{Cs+})$. Thus, using the theory of sec-voltage balance, we have

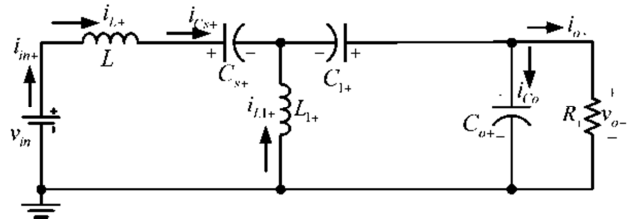
$$DTV_{in} = (1-D)T(V_{Co+} - V_{C1+} - V_{in} + V_{Cs+})$$

or

$$DTV_{in} = (1-D)T(V_{o+} - V_{in}) \tag{5}$$



(a)



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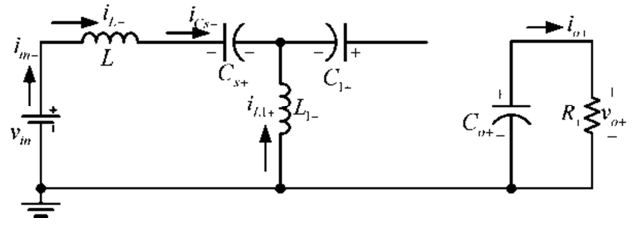


(c)

Figure 2. *Equivalent circuits of positive conversion path. (a) equivalent circuit while turning-on. (b) equivalent circuit while turning-off. (c) equivalent circuit during DCM.*

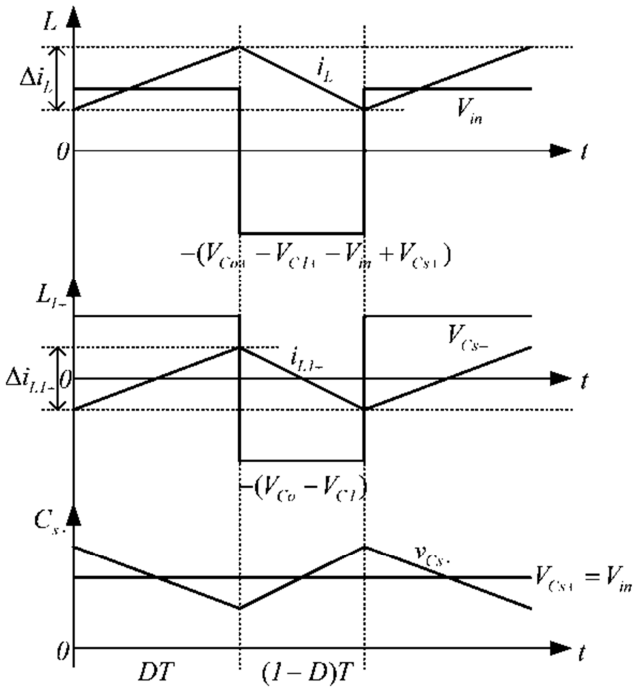


Figure 3. *Positive path: waveforms with enlarged variations.*

Thus,

$$V_{o+} = \frac{1}{1-D} V_{in} \tag{6}$$

In CCM, the voltage transfer gain is

$$M_{S+} = \frac{V_{o+}}{V_{in}} = \frac{1}{1-D} \tag{7}$$

Moreover, the input current is

$$I_{in+} = \frac{1}{1-D} I_{o+} = I_{L+} = I_{Cs+(off)} \tag{8}$$

During switching-off, the charge of C_{o+} and C_{s+} increases, while during switching-on, it decreases. The results we get are

$$\begin{aligned} Q_{Co+(on)} &= I_{o+}DT & Q_{Cs+} &= I_{Cs+(on)}DT \\ Q_{Co+(off)} &= I_{Co+(off)}(1-D)T & Q_{Cs-} &= I_{Cs+(off)}(1-D)T \end{aligned} \tag{9}$$

In the course of a switching cycle, $Q_{Co+(on)} = Q_{Co+(off)}$ and $Q_{Cs+(on)} = Q_{Cs+(off)}$. Therefore,

$$I_{Co+(off)} = \frac{D}{1-D} I_{o+}, I_{Cs+(on)} = \frac{1}{D} I_{o+} \tag{10}$$

While switching-off, $i_{Do+}=i_{Co+}+ i_{o+}$. Therefore,

$$I_{Do+(off)} = I_{Co+(off)} + I_{o+} = \frac{1}{1-D} I_{o+} \tag{11}$$

While switching-off, L_{1+} and C_{1+} form a path along which stored energy is released and transferred to D_o. Thus,

$$I_{C1+(off)} = I_{Do(off)} = \frac{1}{1-D} I_{o+} \tag{12}$$

In a switching cycle, $Q_{C1+(on)} = Q_{C1+(off)}$. Thus,

$$I_{C1+(on)} = \frac{1-D}{D} I_{C1+(off)} = \frac{1}{D} I_{o+} \tag{13}$$

During the turn-on process, L_{1+} and C_{1+} are connected in parallel, and they receive stored energy from C_{s+}. Therefore, according to the KCL law,

$$I_{L1+} = I_{Cs+(on)} - I_{C1+(on)} = 0 \tag{14}$$

Equation (14) is used to calculate the average of the switching cycles under steady-state conditions. It is important to note that the instantaneous inductor current i_{L1+} does flow through L_{1+} during each cycle, and the energy storage and transfer of L_{1+} is achieved by the oscillation of i_{L1+}.

Since the peak-to-peak current change of i_L, Δi_L is equal to DTV_{in} / L, the current change ratio of i_L equals

$$\varsigma_L = \frac{\Delta i_L / 2}{I_L} = \frac{D}{2M_{S+}^2} \frac{R_+}{fL} \tag{15}$$

The current fluctuation during switching-off is equal to Δi_{L1+}, and Δi_{L1+} equals DTV_{in} / L_{1+}. Consequently, the i_{Do} variation ratio is

$$\xi_{Do} = \frac{\Delta i_{L1+} / 2}{I_{Do(off)}} = \frac{D}{2M_{S+}^2} \frac{R_+}{fL_{1+}} \tag{16}$$

The voltage variation of v_{o+} from peak to peak Δv_{o+} is equal to $I_{o+} DT / C_{o+}$. Consequently, the v_{o+} variation ratio is

$$\varepsilon_S = \frac{\Delta v_{o+} / 2}{V_{o+}} = \frac{D}{2R_+ C_{o+} f} \tag{17}$$

2.2. Negative Conversion Path

When switch S is on, D_f is off, and D_{1-} is on. Upon switching-off of S, D_{1-} becomes inactive, and D_f is activated. C_{1-} exhibits traits to elevate the output capacitor voltage by means of the capacitor voltage. The respective equivalent circuits of the negative path during switching-on, switching-off, and DCM are depicted in Figure 4(a-c).

Figure 5 displays switching diagrams with primary steady-state waveforms; Figure 1 refers to the reference directions. The average voltage across a period of time is zero in the steady state. Consequently

$$V_{C1-} = V_{Co-} = V_{o-} \tag{18}$$

V_{C1-} is equal to the voltage across C_{s-} during the switch-on phase. Given that C_{s-} and C_{1-} and are big enough, we have:

$$V_{Cs-} = V_{C1-} = V_{o-} \tag{19}$$

When turning on, the inductor current i_L rises, and when turning off, it falls. V_{in} and $-(V_{Cs-} - V_{in})$ are the corresponding voltages across L. Thus, if we apply the principle of inductor volt-second balancing to L, we obtain

$$DTV_{in} = (1-D)T(V_{Cs-} - V_{in})$$

or

$$DTV_{in} = (1-D)T(V_{o-} - V_{in}) \tag{20}$$

Hence

$$V_{o-} = \frac{1}{1-D} V_{in} \tag{21}$$

In CCM, the voltage transfer gain is

$$M_{S-} = \frac{V_{o-}}{V_{in}} = \frac{1}{1-D} \tag{22}$$

Furthermore, the input current is

$$I_{in} = \frac{1}{1-D} I_{o-} = I_L = I_{Df-off} \tag{23}$$

As a lowpass filter, C_o ensures that

$$I_{L1-} = I_{o-} \tag{24}$$

Since the peak-to-peak current fluctuation of i_L, Δi_L equals to DTV_{in} / L, the variation ratio of i_L is

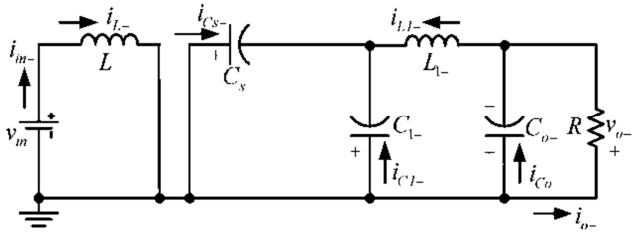
$$\varsigma_L = \frac{\Delta i_L / 2}{I_L} = \frac{D}{2M_{S-}^2} \frac{R_-}{fL} \tag{25}$$

The voltage variation ratio of v_{C1-}, from peak to peak, Δv_{C1-} is approximate to

$$\Delta v_{C1-} = \frac{I_{o-}(1-D)T}{C_{1-}} \tag{26}$$

Consequently, the variation ratio of v_{C1-} is

$$\varepsilon_{C1-} = \frac{\Delta v_{C1-} / 2}{V_{C1-}} = \frac{1}{2M_{S-} f R_- C_{1-}} \tag{27}$$



(a)

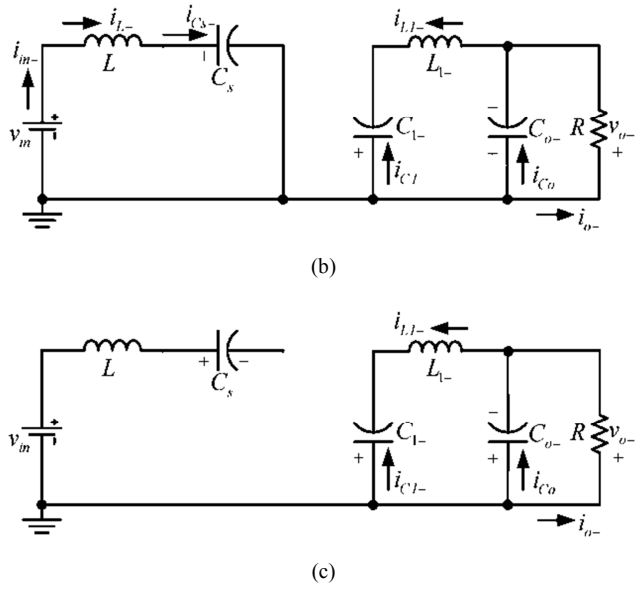


Figure 4. *Equivalent circuits of negative conversion path. (a) equivalent circuit while turning-on. (b) equivalent circuit while turning-off. (c) equivalent circuit during DCM.*

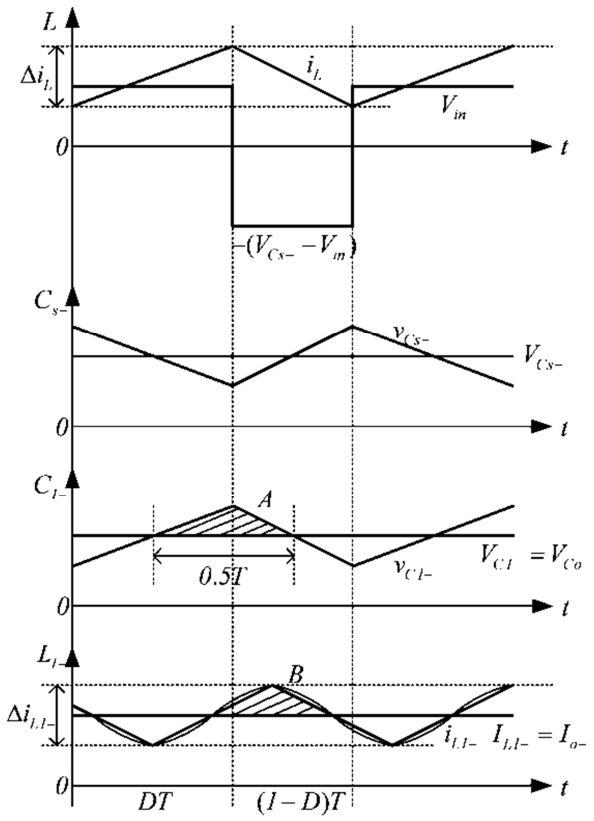


Figure 5. *Negative path: waveforms with enlarged variations.*

Since v_{o-} fluctuates relatively little, the peak-to-peak current variation of i_{L1-} may be computed using the area A of a triangle of width T/2 and height $\Delta v_{C1-}/2$, which is roughly

$$\Delta i_{L1-}=\frac{\frac{1}{2}\frac{\Delta V_{C1-}}{2}\frac{T}{2}}{L_{1-}}=\frac{(1-D)I_{o-}}{8f^2L_{1-}C_{1-}} \tag{28}$$

As a result, the i_{L1-} variation ratio is about equal to

$$\varsigma_{L1-}=\frac{\Delta i_{L1-}/2}{I_{L1-}}=\frac{1}{16M_{S-}f^2L_{1-}C_{1-}} \tag{29}$$

During switching-off the variation of i_{Df} equals to Δi_L, so the variation ratio of i_{Df} is

$$\xi_{Df}=\varsigma_L=\frac{D}{2M_{S-}^2}\frac{R_-}{fL} \tag{30}$$

Because of how tiny the ripple of i_{L1-} is, we consider it as a triangle waveform in Figure 5 to make the computation simpler. Therefore, area B, is used to determine the peak-to-peak voltage variation of v_{o-}, which is roughly

$$\Delta v_{o-}=\frac{\frac{1}{2}\frac{\Delta i_{L1-}}{2}\frac{T}{2}}{C_{o-}}=\frac{(1-D)I_{o-}}{64f^3L_{1-}C_{1-}C_{o-}} \tag{31}$$

Consequently, the variation ratio of v_{o-} is almost equal to

$$\varepsilon_S=\frac{\Delta v_{o-}/2}{V_{o-}}=\frac{1}{128M_{S-}f^3L_{1-}C_{1-}C_{o-}R_-} \tag{32}$$

The definitions of $V_o=V_{o+}=|V_{o-}|$, $M_S=M_{S+}=M_{S-}=V_o/V_{in}=1/(1-D)$, and the mirror-symmetrical double output voltages in CCM can be found from (7) and (22). Table 1 provides a summary of the voltage and current strains experienced by each semiconductor in the CCM.

Table 1. *Summary of voltage and current stresses.*

	Voltage Stress	Current Stress
S	$\frac{1}{1-D}V_{in}$	$\frac{1+2D-D^2}{D(1-D)}I_o$
D_o		$\frac{1}{1-D}I_o$
D_{1+}		$\frac{1}{D}I_o$
D_f		$\frac{1}{1-D}I_o$
D_{1-}		I_o

2.3. DCM

The converter is in DCM mode when the free wheeling diode currents i_{Do} and i_{Df} reach zero during switch off before the start of the subsequent switching cycle. Figures 2(c) and 4(c) depict the corresponding circuits for the DCM operation, respectively. We deliberately choose $L=L_{1+}$ and $R_+=R_-$ in order to produce the mirror-symmetrical Dual-Output voltages in DCM. Z_{N+} represents the normalized load for the positive conversion path, $R_+/(fL_{1+})$, and $R_-/(fL)$ represents the normalized load for the negative conversion path, Z_{N-}. We therefore define $Z_N=Z_{N+}=Z_{N-}$ and $\xi=\xi_{Do}=\xi_{Df}$. DCM requires condition $\xi\geq 1$, i.e.

$$\xi = \frac{D}{2M_S^2} Z_N \geq 1 \tag{33}$$

In the rare event that i_{Do} and i_{Df} both drop to zero at t = T, the circuit functions at the intersection of CCM and DCM. As a result, the following is the boundary between CCM and DCM:

$$Z_{N-B} = \frac{2M_S^2}{D} = \frac{2}{D(1-D)^2} \tag{34}$$

The circuit runs in DCM when $Z_N > Z_{N\text{-}B}$. At $t = t_{1+} = [D+m_{S+}(1\text{-}D)]\ T$, where i_{Do} drops to zero under the DCM condition,

$$DT < t_1 < T \quad \text{and} \quad 0 < m_{S+} < 1$$

In this case, m_{S+}, which is the present filling efficiency for the positive conversion path, is defined as

$$m_{S+} = \frac{t_1 - DT}{(1-D)T} \tag{35}$$

In DCM, i_L rises throughout the on-time phase and falls between DT and $m_{S+}(1\text{-}D)T$. V_{in} and $-(V_{o+} - V_{in})$ are the corresponding voltages across L for the positive conversion routes. Therefore, applying the theory of volt-second balancing, we have

$$DTV_{in} = m_{S+}(1-D)T(V_{o+} - V_{in}) \tag{36}$$

Furthermore, while switching-off, the transferred charges of L_{1+} equals to $m_S(1-D)T\Delta i_{L1+}/2$, which offsets the entire amount of charges of the load. Thus, we have

$$I_{o+}T = \frac{1}{2} m_{S+}(1-D)T\Delta i_{L1}$$

or

$$\frac{V_{o+}}{R_+} T = \frac{1}{2} m_{S+}(1-D)T \frac{DTV_{in}}{L_{1+}} \tag{37}$$

Combining (36) and (37), we acquire

$$m_{S+} = \frac{1+\sqrt{1+2D^2Z_N}}{D(1-D)Z_N} \tag{38}$$

From (36), we obtain

$$V_{o+} = [1 + \frac{D}{m_{S+}(1-D)}]V_{in} \tag{39}$$

Consequently, the following positive voltage transfer gain in DCM is obtained by replacing (38) with (39):

$$M_{S+(DCM)} = \frac{1}{2}(1+\sqrt{1+2D^2Z_N}) \tag{40}$$

i_{Df} drops to zero under the DCM condition at $t = t_{1-} = [D+m_{S-}(1\text{-}D)]T$, where $DT < t_1 < T$ and $0 < m_{S-} < 1$

The current filling efficiency for the negative conversion path, m_{S-}, denoted as

$$m_{S-} = \frac{t_1 - DT}{(1-D)T} \tag{41}$$

V_{in} and $-(V_{o-} - V_{in})$ are the corresponding voltages across L for the negative conversion routes. Thus, using the volt-second balance concept, we have

$$DTV_{in} = m_{S-}(1-D)T(V_{o-} - V_{in}) \tag{42}$$

Furthermore, upon switching-off, the transferred charges of L to the positive conversion path equal $m_{S-}(1-D)T\Delta i_L/2$, which makes up for the whole amount of charges used by the load. Thus, we have

$$I_{o-}T = \frac{1}{2} m_{S-}(1-D)T\Delta i_L$$

or

$$\frac{V_{o-}}{R_-} T = \frac{1}{2} m_{S-}(1-D)T \frac{DTV_{in}}{L} \tag{43}$$

Combining (42) and (43), we obtain

$$m_{S-} = \frac{1+\sqrt{1+2D^2Z_N}}{D(1-D)Z_N} \tag{44}$$

From (42), we have

$$V_{o-} = [1 + \frac{D}{m_{S-}(1-D)}]V_{in} \tag{45}$$

Consequently, the negative voltage transfer gain in DCM that results from changing (44) into (45) is as follows:

$$M_{S-(DCM)} = \frac{1}{2}(1+\sqrt{1+2D^2Z_N}) \tag{46}$$

We can determine that $m_S = m_{S+} = m_{S-}$, $m_S = m_{S+} = m_{S-}$, $V_o = V_{o+} = |V_{o-}|$, $M_{S(DCM)} = M_{S+(DCM)} = M_{S-(DCM)} = V_o/V_{in} = (1+\sqrt{1+2D^2Z_N})/2$ and the mirror-symmetrical double output voltages in DCM are acquired from the study above. The boundary curve between CCM and DCM and the voltage transfer gains vs the normalized load are obtained using (7), (22), (34), (40) and (46), as seen in Figure 6. The circuit design's essential parameters and output performance can be estimated using equations (17), (32), and Figure 6. It is evident that a higher output voltage in DCM could result from a bigger normalized load. In the presence of condition D = 1/3, the minimal Z_N value at the boundary is 13.5. This indicates that the highest likelihood of this converter entering DCM is in condition D = 1/3.

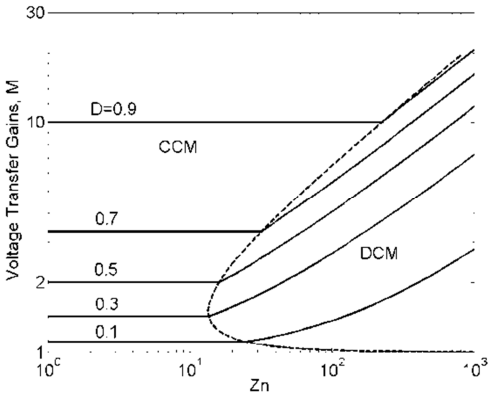


Figure 6. *Proposed topology: boundary between CCM and DCM, and voltage transfer gains against Z_N.*

3. Boost Enhanced Series

The Dual-Output mirror-symmetrical VL-type converter serves as the foundation for all of the circuits in the boost improved series. Using the voltage lift technique, we can build corresponding enhanced circuits since the positive and negative conversion channels in Figure 1 share a similar source section, which may be thought of as a boost converter circuit. Several new circuits are applied to the source section, increasing V_{Cs+} and V_{Cs-} step by step along the geometric progression and transferring significantly more energy to C_{s+} and C_{s-} in each cycle. We refer to them as boost[1], boost[2], and boost[M] improved circuits, respectively, to make things easier to understand.

3.1. Boost[1] Enhanced Circuit

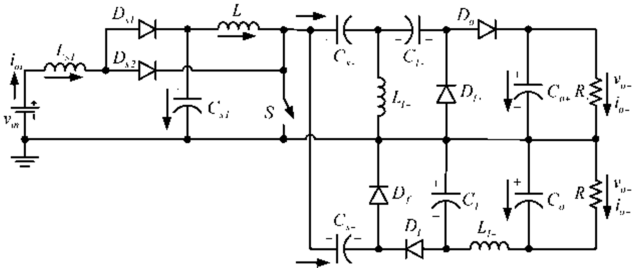


Figure 7. *Boost enhanced series: boost1 enhanced circuit.*

As illustrated in Figure 7, the components (L_{s1}-D_{s1}-D_{s2}-C_{s1}), denoted by *boost[1]*, constitute a basic VL cell and are added to the source section. Using the additional components, the newly-derived architecture in Figure 7 offers a single boost circuit augmentation. D_{s1} is off and D_{s2} is on when S is turned on. D_{s1} is on and D_{s2} is off when S turns off. By acting according to its properties, the capacitor C_{s1} raises the source voltage V_{in}. Consequently,

$$V_{Cs1} = \frac{1}{1-D} V_{in} \tag{47}$$

In every cycle, energy from C_{s1} is transferred to C_{s+} and C_{s-}. Moreover, there is a notable increase in V_{Cs+} and V_{Cs-}. As a result, we obtain

$$\begin{cases} V_{Cs+} = V_{Cs1} = \dfrac{1}{1-D} V_{in} \\ V_{Cs-} = \dfrac{1}{1-D} V_{Cs1} = \dfrac{1}{(1-D)^2} V_{in} \end{cases} \tag{48}$$

Consequently, the voltage transfer gains of the boost[1] improved circuit in CCM are as follows, derived from the previously mentioned analysis and computation in Sections II and III:

$$\begin{cases} M_{boost^1+} = \dfrac{V_{o+}}{V_{in}} = \dfrac{1}{(1-D)^2} \\ M_{boost^1-} = \dfrac{V_{o-}}{V_{in}} = -\dfrac{1}{(1-D)^2} \end{cases} \tag{49}$$

Comparably, the boost[1] improved circuit in DCM has the following voltage transfer gains:

$$\begin{cases} M_{boost^1+(DCM)} = \dfrac{V_{o+}}{V_{in}} = \dfrac{(1+\sqrt{1+2D^2 Z_N})}{2(1-D)} \\ M_{boost^1-(DCM)} = \dfrac{V_{o-}}{V_{in}} = -\dfrac{(1+\sqrt{1+2D^2 Z_N})}{2(1-D)} \end{cases} \tag{50}$$

3.2. Boost[M] Enhanced Circuit

With reference to Figure 7, by iteratively repeating the components (L_{s1}-D_{s1}-D_{s2}-C_{s1}), the boost[M] enhanced circuit (i.e. multiple boost circuits enhancement) can be realized in the source part. Assuming n voltage lift cells, Figure 8 depicts the generalized form of the boost enhanced series for the mirror-symmetrical Dual-Output VL-type converter. Figure 8 shows the generalized form of the boost enhanced series for the mirror-symmetrical Dual-Output VL-type converter. The power switch S is shared by all circuits, simplifying the control method and cutting costs dramatically. As a result, there are ($2n$+4) diodes, (n+3) inductors, (n+6) capacitors, and one switch in every circuit. Every capacitor has an adequate size. Every cycle, energy from C_{sn} is transferred to C_{s+} and C_{s-}, increasing V_{Cs+} and V_{Cs-}.

$D_{s(2j)}$ is on, and $D_{s(2j-1)}$ is off in the j^{th} cell of the source section when switch S is turned on. $D_{s(2j)}$ is off and $D_{s(2j-1)}$ is on when S turns off. Thus, we obtain:

$$V_{Csn} = \frac{1}{(1-D)^n} V_{in} \tag{51}$$

$$\begin{cases} V_{Cs+} = V_{Csn} = \dfrac{1}{(1-D)^n} V_{in} \\ V_{Cs-} = \dfrac{1}{1-D} V_{Csn} = \dfrac{1}{(1-D)^{n+1}} V_{in} \end{cases} \tag{52}$$

Consequently, based on the analysis and computation done previously, the general voltage transfer gains of the boost series are:

$$\begin{cases} M_{boost^M-S+} = \dfrac{V_{o+}}{V_{in}} = \dfrac{1}{(1-D)^{n+1}} \\ M_{boost^M-S-} = \dfrac{V_{o-}}{V_{in}} = -\dfrac{1}{(1-D)^{n+1}} \end{cases} \tag{53}$$

Comparably, the boost series' overall voltage transfer improvements in DCM are:

$$\begin{cases} M_{boost^M+(DCM)} = \dfrac{V_{o+}}{V_{in}} = \dfrac{(1+\sqrt{1+2D^2Z_N})}{2(1-D)^n} \\ M_{boost^M-(DCM)} = \dfrac{V_{o-}}{V_{in}} = -\dfrac{(1+\sqrt{1+2D^2Z_N})}{2(1-D)^n} \end{cases} \tag{54}$$

The Dual-Output mirror-symmetrical voltages in CCM and DCM are observed to be produced from (53) and (54).

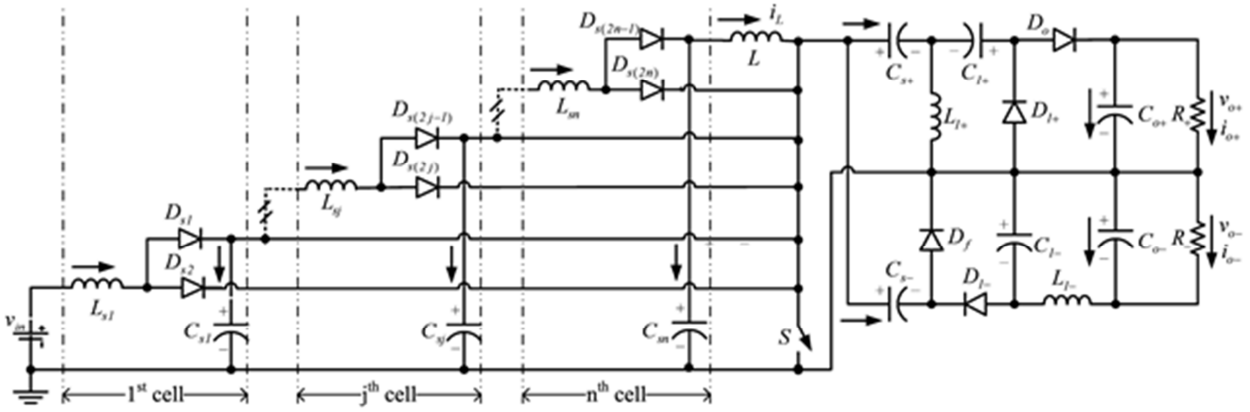


Figure 8. *Generalized representation of the boost enhanced series (the boost^M enhanced circuit).*

4. Super Enhanced Series

Every circuit in the super enhanced series comes from the matching circuits in the boost series that are suggested in the section above. Several new circuits are applied to the source section, increasing V_{Cs+} and V_{Cs-} step by step along the geometric progression and transferring significantly more energy to C_{s+} and C_{s-} in each cycle. To make things easier to understand, we refer to them as *super*^{1}, *super*^{2} and *super*^{M} improved circuits, respectively, because they can deliver greater voltage transfer improvements than the boost series.

4.1. Super^1 Enhanced Circuit

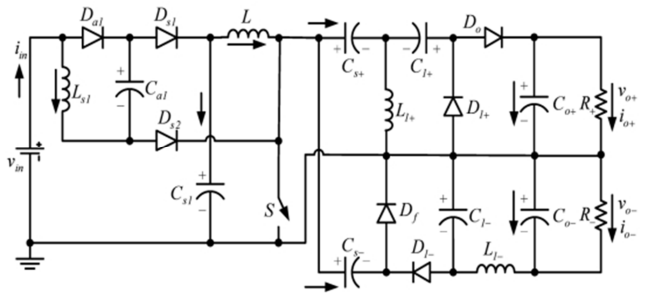


Figure 9. *Super enhanced series: super^1 enhanced circuit.*

This circuit is a simple voltage super lift cell that is created by adding one diode and one capacitor (D_{a1}-C_{a1}) to the boost^1 circuit. In Figure 9, the circuit diagram is displayed. D_{s1} is off and D_{s2} and D_{a1} are on when switch S is turned on. D_{s1} is on and D_{s2} and D_{a1} are off when S turns off. V_{Cs1} are elevated by V_{Ca1} because C_{a1} links L_{s1} and C_{s1} during switching-off by acting as a ladder joint.

Therefore,

$$V_{Cs1} = \frac{1}{1-D}V_{in} + V_{Ca1} = \frac{2-D}{1-D}V_{in} \tag{55}$$

The energy is transferred to C_{s+} and C_{s-} in each cycle from C_{s1}. In every cycle, energy from C_{s1} is transferred to C_{s+} and C_{s-}.

Moreover, there is a notable increase in V_{Cs+} and V_{Cs-}. We obtain

$$\begin{cases} V_{Cs+} = V_{Cs1} = \dfrac{2-D}{1-D}V_{in} \\ V_{Cs-} = \dfrac{1}{1-D}V_{Cs1} = \dfrac{2-D}{(1-D)^2}V_{in} \end{cases} \tag{56}$$

Consequently, the voltage transfer gains of the super^1 improved circuit in CCM are as follows, derived from the previously mentioned analysis and computations in Sections II and III:

$$\begin{cases} M_{\text{super}^1+} = \dfrac{V_{o+}}{V_{in}} = \dfrac{2-D}{(1-D)^2} \\ M_{\text{super}^1-} = \dfrac{V_{o-}}{V_{in}} = -\dfrac{2-D}{(1-D)^2} \end{cases} \tag{57}$$

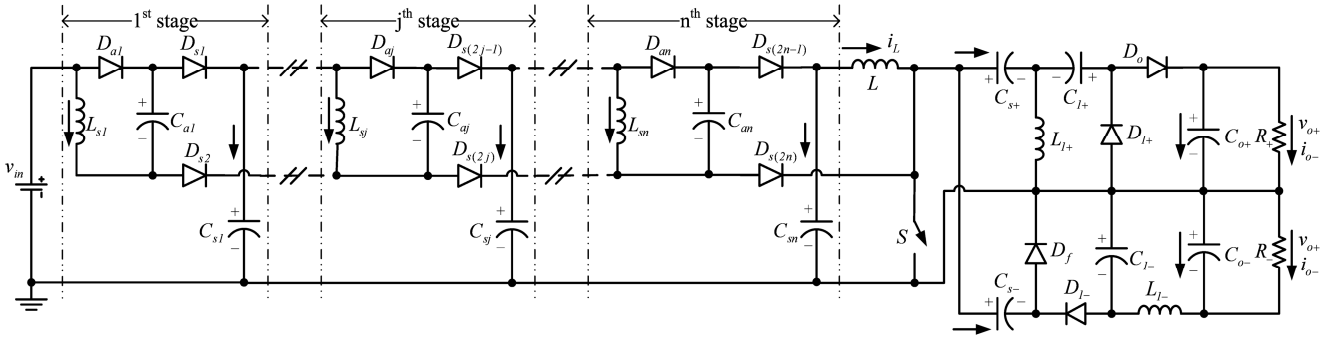


Figure 10. *Generalized representation of the super enhanced series (the super^M enhanced circuit).*

Comparatively, the super^1 improved circuit in DCM has the following voltage transfer gains:

$$\begin{cases} M_{\text{super}^1+(DCM)} = \dfrac{V_{o+}}{V_{in}} = \dfrac{(2-D)(1+\sqrt{1+2D^2Z_N})}{2(1-D)} \\ M_{\text{super}^1-(DCM)} = \dfrac{V_{o-}}{V_{in}} = -\dfrac{(2-D)(1+\sqrt{1+2D^2Z_N})}{2(1-D)} \end{cases} \tag{58}$$

4.2. Super^M Enhanced Circuit

By repeating the components (L_{s1}-D_{a1}-C_{a1}-D_{s1}-D_{s2}-C_{s1}), the super^M improved circuit can be built, as shown in Figure 9. Figure 10 shows the generalized form of the super enhanced series for the mirror-symmetrical Dual-Output VL-type converter, assuming that there are n voltage super lift cells. Since every circuit uses the same power switch S, the control system is made much simpler and costs much less. As a result, each circuit contains one switch, (*3n+4*) diodes, (2n+6) capacitors, and (n+3) inductors. Every capacitor has an adequate size. Every cycle, energy from C_{sn} is transferred to C_{s+} and C_{s-}, which can greatly increase V_{Cs+} and V_{Cs-}.

When switch S is activated in the j^{th} cell of the source section, $D_{s(2j)}$ and D_{aj} are turned on while $D_{s(2j-1)}$ is turned off. $D_{s(2j)}$ and D_{aj} are off and $D_{s(2j-1)}$ is on when S turns off. The generic formulas for all super^M improved circuits can be found as follows from the analysis and computation above:

$$V_{Csn} = (\frac{2-D}{1-D})^n V_{in} \tag{59}$$

$$\begin{cases} V_{Cs+} = V_{Csn} = (\dfrac{2-D}{1-D})^n V_{in} \\ V_{Cs-} = \dfrac{1}{1-D} V_{Csn} = \dfrac{(2-D)^n}{(1-D)^{n+1}} V_{in} \end{cases} \tag{60}$$

Consequently, the general voltage transfer gains of the super enhanced series in CCM are as follows, based on the previously mentioned analysis and computation in Sections II and III:

$$\begin{cases} M_{\text{super}^M+} = \dfrac{V_{o+}}{V_{in}} = \dfrac{(2-D)^n}{(1-D)^{n+1}} \\ M_{\text{super}^M-} = \dfrac{V_{o-}}{V_{in}} = -\dfrac{(2-D)^n}{(1-D)^{n+1}} \end{cases} \tag{61}$$

In a similar vein, the super enhanced series' overall voltage transfer increases in DCM are:

$$\begin{cases} M_{\text{super}^M+(DCM)} = \dfrac{V_{o+}}{V_{in}} = \dfrac{(1+\sqrt{1+2D^2Z_N})}{2}(\dfrac{2-D}{1-D})^n \\ M_{\text{super}^M-(DCM)} = \dfrac{V_{o-}}{V_{in}} = -\dfrac{(1+\sqrt{1+2D^2Z_N})}{2}(\dfrac{2-D}{1-D})^n \end{cases} \tag{62}$$

The mirror-symmetrical Dual-Output voltages in CCM and DCM are observed to be produced from (61) and (62).

5. Simulation and Experimental Results

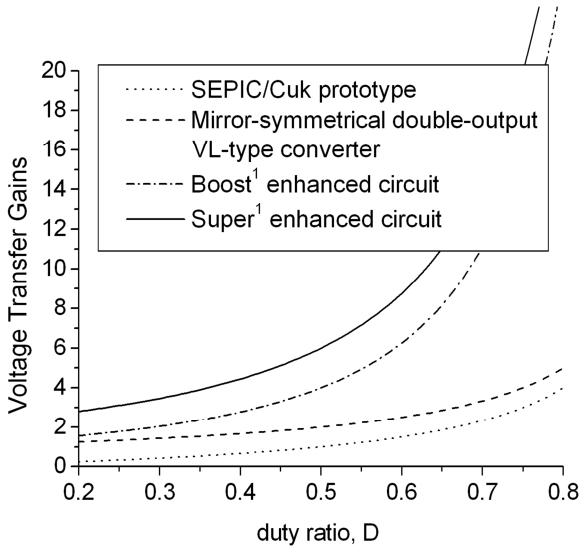


Figure 11. *Output voltages transfer gains of the proposed topologies.*

Figure 11 displays the voltage transfer gains of the three suggested topologies in CCM and compares them to the traditional SEPIC and Cûk converters. Three distinct situations were examined using the PSIM simulation program. To validate the theoretical study, the voltages of the positive and negative routes are provided. In order to match the simulation results with the hardware testing circuits, the relevant designs were also built. It is observed that the oscillograph's channels 1 and 2 (which share the common ground) exhibit v_{o+} and v_{o-}, respectively.

5.1. Simulation and Experimental Results of the Dual-Output VL-Type Converter

The circuit settings for the simulation, as shown in Figure 1, are as follows: $V_{in}=10V$, $R_+ = R_- =100\Omega$, $L=1mH$, $L_{1+}=L_{1-}=500\mu H$, $C_{1+}=C_{1-}=22\mu F$, $C_{s+}=C_{s-}=110\mu F$, $C_{o+}=C_{o-}=47\mu F$, $D=0.5$ and $f=100kHz$. Since the case must be completed in CCM, we apply (34) to obtain the normalized load boundary values. In this instance, the normalized loads Z_{N+} and Z_{N-} are situated at the boundary curve's left CCM region, as depicted in Figure 6. It follows that the aforementioned parameters are suitable for the CCM functioning. We derive the Dual-Output voltage V_{o+} and V_{o-} theoretical values in accordance with (7) and (22). They are equivalent to -20V and 20V, in that order. Figure 12 displays the results of the simulation run in Psim with zero beginning circumstances. Curve 1 represents v_{o+} in the positive conversion route, while curve 2 represents v_{o-} in the negative. It is evident that the startup procedure is rapid and comparable to that of other dc-dc converters currently in use. The theoretical analysis and the simulation's steady-state values match exactly.

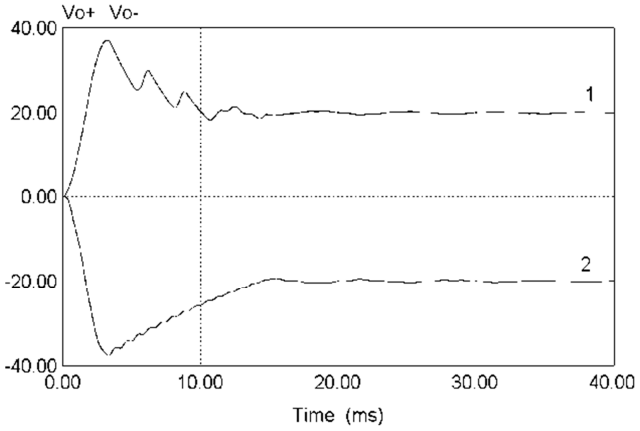


Figure 12. *Simulation results of the mirror-symmetrical Dual-Output VL-type converter.*

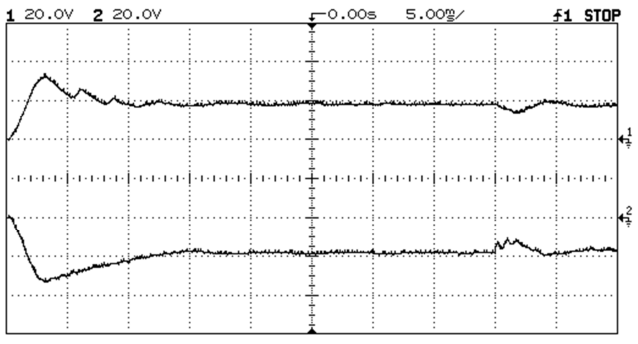


Figure 13. *Experimental results of the mirror-symmetrical Dual-Output VL-type converter.*

The testing hardware circuit is built using the same settings, and Figure 13 displays the experimental startup curves. With 20V/Div, the curve seen in Channel 1 represents positive output v_{o+}, or around 18.7V in the steady state. In Channel 2, the curve exhibiting 20V/Div is indicative of the negative output v_{o-}, which in a steady condition is likewise around 18.7V. We can observe that the observed findings agree extremely well with the theoretical analysis and simulation results when taking into account the effects induced by the parasitic factors. In addition, a load change from 100Ω to 33Ω in the negative conversion path is made to observe its dynamics. It is seen that both output voltages can recovery their steady states after several milliseconds.

5.2. Simulation and Experimental Results of the Boost[1] Enhanced Circuit

The circuit settings for the simulation, as shown in Figure 7, are as follows: $V_{in}=10V$, $R_+ = R_- =100\Omega$, $L_{s1}=L=1mH$, $L_{1+}=L_{1-}=500\mu H$, $C_{s1}=C_{1+}=C_{1-}=22\mu F$, $C_{s+}=C_{s-}=110\mu F$, $C_{o+}=C_{o-}=47\mu F$, $D=0.5$ and $f=100kHz$. We derive the theoretical Dual-Output voltage V_{o+} and V_{o-} values in accordance with (49). They are, thus, equivalent to 40V and -40V. Figure 14 displays the results of the Psim simulation. Curve 1 represents v_{o+} in the positive conversion path, and curve 2 represents v_{o-} in the negative conversion path. It can be observed that the simulation's steady-state values perfectly match the results of the theoretical study.

The testing hardware circuit is built using the same parameters, and the related experimental curves are displayed in Figure 15 accordingly. When 20V/Div is used, the curve in Channel 1 represents positive output v_{o+}, or around 37V in a steady condition. In Channel 2, the curve displaying 20V/Div is indicative of the negative output v_{o-}, which in a steady condition is likewise approximately 37V. We can observe that the observed results agree extremely well with the theoretical analysis and simulation results when taking into account the effects induced by the parasitic factors.

5.3. Simulation and Experimental Results of the Super[1] Enhanced Circuit

With reference to Figure 9, the simulation's circuit settings are as follows: $V_{in}=10V$, $R_+ = R_- =100\Omega$, $L_{s1}=L=1mH$, $L_{1+}=L_{1-}=500\mu H$, $C_{s1}=C_{1+}=C_{1-}=22\mu F$, $C_a=220\mu F$, $C_{s+}=C_{s-}=110\mu F$, $C_{o+}=C_{o-}=47\mu F$, $D=0.5$ and $f=50kHz$. We derive the theoretical Dual-Output voltage V_{o+} and V_{o-} values from (57). They are, thus, equivalent to 60V and -60V. Figure 16 displays the results of the Psim simulation. Curve 1 represents v_{o+} in the positive conversion path, and curve 2 represents v_{o-} in the negative conversion path. The theoretical analysis and the simulation's steady-state values match exactly.

The hardware circuit for testing is built using the same specifications. Figure 17 displays the relevant experimental curves, respectively. When 20V/Div is used, the curve in Channel 1 represents positive output v_{o+}, or around 54V in a steady condition. With 20V/Div, the curve displayed in Channel 2 represents the negative output v_{o-}, which in a steady condition is likewise roughly 54V. We can observe that the observed results agree extremely well with the theoretical

analysis and simulation results when taking into account the effects induced by the parasitic factors.

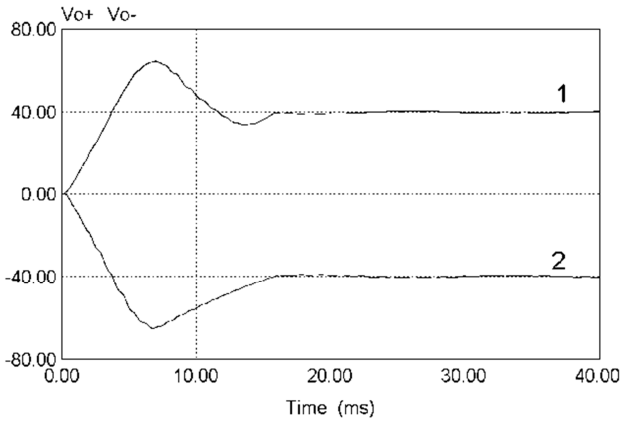


Figure 14. *Simulation verification for the boost[1] enhanced circuit.*

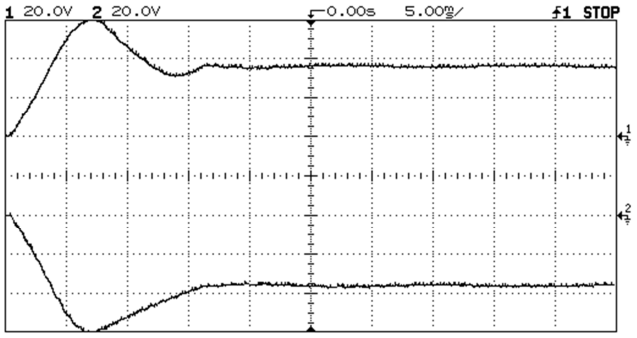


Figure 15. *Experimental verification for the boost[1] enhanced circuit.*

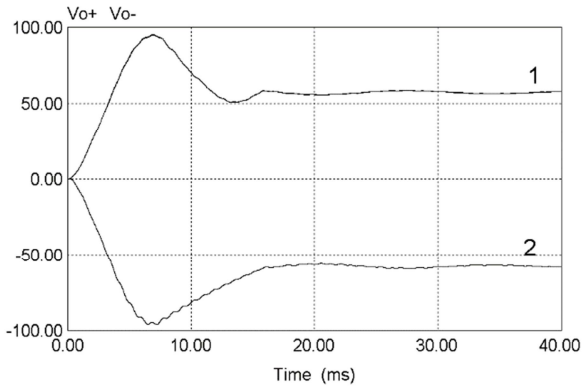


Figure 16. *Simulation verification for the super[1] enhanced circuit.*

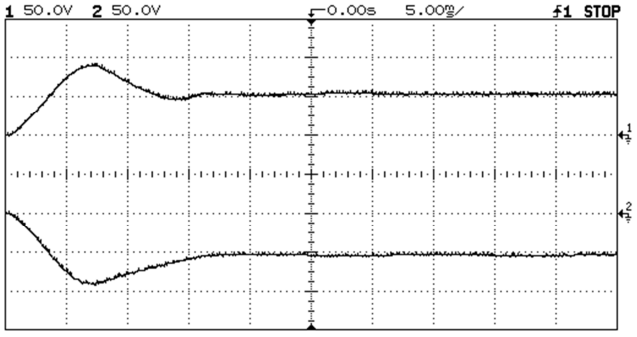


Figure 17. *Experimental verification for the super[1] enhanced circuit.*

5.4. Transient Modelling, Stability Analysis and Control Strategy

As seen in Figures 12–17, the open-loop transient processes are extremely rapid, taking only a few milliseconds, and they display the typical traits found in dc–dc converters. High order models can be derived for all suggested converters using state-space averaging and switching flow graph methods, whereas reduced order models can be derived using the energy factor method [18]. Due to the length constraints of the paper, it is challenging to describe in this one. In subsequent articles, we would want to present the comprehensive transient process and circuit stability analysis.

A quick overview of the control strategy is provided below for the benefit of future research and application. Two primary issues should be taken into account in the control method for the suggested converters. One way is to regulate the single switch to provide the mirror-symmetrical Dual-Output voltages. The other is to remove the positive and negative output voltage imbalance caused by mismatched capacitance or shifting loads. It is evident from every suggested topology that if S is off, the negative v_{o-} will diminish and if S is on, the positive v_{o+} would decrease. Consequently, the phenomenon of complimentary output voltage variation can be employed to eradicate the imbalance caused by Dual-Output voltages. With the general control technique shown in Figure 18, both of these can be satisfied.

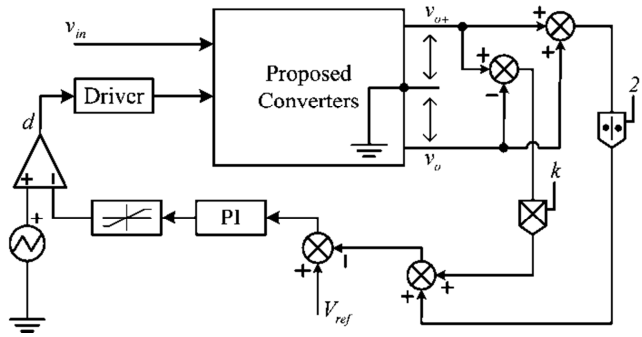


Figure 18. *General voltage-mode control strategy of the proposed converters.*

The conventional voltage-mode PI controller serves as the foundation for the suggested control technique. The PI controller now includes the imbalance error in addition to the average output voltage. The controller is applied to the topology in Figure 1 in order to verify the suggested approach. The circuit specifications match those found in Section V.A. The controller's parameters are as follows: k=1, the PI unit's gain of 0.01; the PI unit's time constant of 0.0017 seconds; and the limiter's maximum limit of 0.8. The curves for v_{o+} and v_{o-} in relation to different load combinations are shown in Figure 19. R+ and R_{-} is initially set to 100Ω, but at t=*40*ms, it changes to 33Ω. It is evident that the single switch's duty ratio has been set at 0.5. Elimination of the high overshot in the transient process and the voltage imbalance in the steady state has occurred. Given that the circuit architectures of all the suggested topologies are identical, the general control method can be applied to all of them. Future studies will examine the additional sophisticated control techniques that can be derived

from the voltage-mode controller.

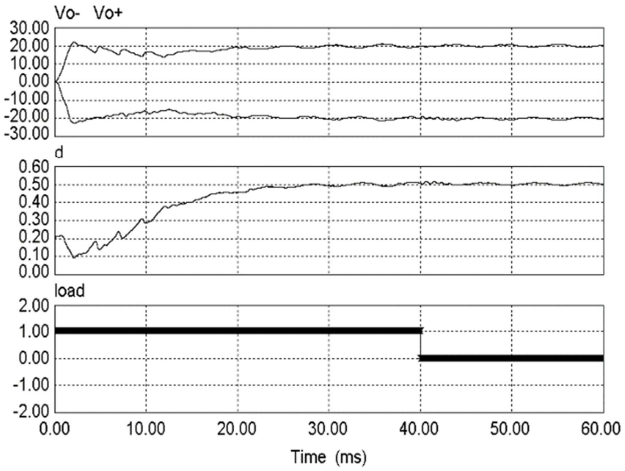


Figure 19. *Verification of the proposed general control strategy.*

6. Conclusions

The use and advancement of the VL approach in the topology creation of Dual-Output dc-dc converters were shown in this study. It has been suggested to build a number of innovative mirror-symmetrical Dual-Output dc-dc converters, which can significantly boost the output voltage transfer gains. The suggested converters prevent taking an excessively high duty ratio and mitigate the effects of parasitic factors. In addition, they have modest ripples in simple structures, a single power switch, and a common ground. A number of significant findings were obtained through theoretical topology research that may find utility in future applications. With careful parameter selection, we may use a positive input source to produce mirror-symmetrical Dual-Output voltages. These converters are suitable for high mirror-symmetrical Dual-Output voltage industrial applications, medical equipment, and computer peripheral circuits.

Conflicts of Interest

The authors declare no conflicts of interest.

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